REMARKS

Favorable consideration of this application is respectfully requested.

Claims 1 – 10 and 36 - 73 are currently active in this case. Claims 11 - 35 have been canceled and Claims 36 – 73 have been added by way of the present amendment. Each new and amended claim is supported by the specification and claims as originally submitted and no new matter has been added.

In the outstanding Official Action, Claims 8 and 33 were rejected under 35 U.S.C. §112, first paragraph as failing to comply with the enablement requirement; Claims 1-4, 6, 7, 10-14, 16-19, 26-29, 31, 32, and 35 were rejected under 35 U.S.C. §102(e) over *Charron* (U.S. Patent No. 6,732,274); Claims 11-14 were rejected under 35 U.S.C. §102(e) over *Habib* (U.S. Patent No. 6,035,368); Claims 5, 20-22, and 30 were rejected under 35 U.S.C. §103(a) over *Charron*; Claims 9 and 34 were rejected under 35 U.S.C. §103(a) over *Charron* in view of *Schlotterer et al.* (U.S. Patent No. 3,827,029, hereinafter *Schlotterer*); Claim 15 was rejected under 35 U.S.C. §103(a) over *Charron* in view of *Brunner* (U.S. Patent No. 4,727,544); Claim 15 was rejected under 35 U.S.C. §103(a) over *Habib* in view of *Brunner*; and Claims 23-25 were rejected under 35 U.S.C. §103(a) over *Schlotterer* in view of *Brunner*.

Applicant respectfully traverses the rejection of Claim 8 as failing to comply with the enablement requirement. As to maintaining control device stability, the present invention is directed to computer memory protection and recites several embodiments in which a control device, such as a microprocessor is deprived access to the memory (e.g., disconnected) in cases where the memory has been breached. However, as noted in Applicants specification, simply removing memory access to a control device can cause the control device to behave erratically (page

18, line 22 – page 19, line 5). The present invention maintains stability by, for example, switching the data bus path to a predetermined pattern (e.g., page 19, lines 7-12, also see Fig. 25 which illustrates steps for placing a predetermined pattern on the data bus). Applicants have further amended the specification to specifically recite the same language/terms used in the claims (see specification amendment submitted herewith for the paragraph on page 53, line 13, the entire original paragraph also recites a similar plan to place predetermined data on the data bus). Therefore, Applicants respectfully submit that the claim language in Claim 8 and original Claim 33 is fully supported in Applicants specification. Accordingly, Applicants respectfully request that the rejection under 35 USC 112, first paragraph be withdrawn.

Applicant respectfully traverses the rejection of Claim 1 as being anticipated by *Charron*. Claim 1 recites:

> ***1. (Original) A method of protecting a program memory device including program memory content, wherein the program memory content is associated with a previously stored signature, the method comprising:***
>
> ***automatically disconnecting the program memory device from a control device that is operationally dependent upon the program memory device;***
>
> ***halting the control device;***
>
> ***verifying whether a present signature is equivalent to the previously stored signature to obtain a verification result; and***
>
> ***based on the verification result, performing one of:***
>
> ***disabling reading and writing of the program memory device; or***

automatically reconnecting the program memory device to the control device.

However, *Charron* fails to teach or suggest similar subject matter.

Applicant respectfully traverses any assertion that equates Applicant's stored signature to *Charron's* stored personality data (random number generated by circuitry and stored in the memory). Applicant respectfully notes Applicant's specification specifically defines signature as a value calculated from the memory content (e.g. page 3, lines 7 – 8, *"generating a signature of the memory contents."*). And, Claim 1 specifically recites program memory content "...associated with a previously stored signature," and verification that "...*a present signature is equivalent to the previously stored signature.*"

In contrast, *Charron's* personality data, while eventually stored in memory content, is neither a signature value nor is it a signature calculated from the memory content. Instead, *Charron's* personality data is based on a random configuration of electrical components (e.g. a configuration of resistors randomly selected upon manufacture of the device (e.g. *Charron*, Fig. 1, #50, col. 3 lines 17–26). Thus, *Charron's* personality data is not the same as a signature and cannot fairly suggest a signature.

Further, Claim 1 specifically recites that the *"program memory content is associated with a previously stored signature."* However, instead of being associated with the program memory content, *Charron's* random number is associated with the random electrical components and then stored as program memory content, but does nothing to verify memory contents as in a signature because it is not associated with the memory contents as claimed.

Therefore, Applicant respectfully submits that Claim 1 cannot be anticipated by *Charron* because *Charron* fails to teach or suggest subject matter specifically claimed in Claim 1. Accordingly, Applicant respectfully submits that Claim 1 is patentable over *Charron*.

Applicants respectfully traverse the rejection of Claim 2 as being anticipated (rejected under 35 USC 102(b)by *Charron*. Claim 2 recites:

> ***2. (Original) The method of Claim 1, wherein the step of verifying comprises:***
>
> ***independently computing a binary content verification of the program memory content; and***
>
> ***comparing the previously stored signature with the binary content verification.***

However, *Charron* fails to teach or suggest similar subject matter.

Applicants respectfully note that *Charron* discloses a conventional program memory and processing device. Upon start-up, *Charron* reads a voltage (e.g., from resistors 50, *Charron*, col. 3, lines 18-25), digitizes the voltage (*Charron*, col. 3, lines 26-29), and then compares the digitized voltage to a value stored in the program memory 28 (*Charron*, col. 3, lines 40-50). Thus, *Charron* reads the resistor value and compares it to a previously stored value. However, Claim 1 recites a step of *"computing,"* and reading an existing voltage is not the same as performing a computation.

Further, Claim 2 specifically recites *"...computing a binary content verification of the program memory content."* However, reading a voltage value only produces a voltage number but is not a computation that verifies the content of the program memory. That the voltage value can be used to verify a previously stored voltage value in a single memory location does not make the voltage value a

computation that verifies the content of the program memory because it is not derived from the program memory and says nothing about the program memory contents save a single previously stored location.

Finally, Applicants respectfully note that *Charron* discloses an ordinary architecture having a memory (EEPROM 28) and microcontroller 25. The EEPROM stores data used by the microcontroller (*Charron*, col. 2, lines 54-57). However, Claim 2 specifically recites *"independently computing a binary content verification of the program memory content,"* and, *Charron's* ordinary architecture does not teach any facilities in which a binary content verification can be independently computed because all computations in *Charron* are performed by and dependent upon a single microcontroller (microcontroller 25).

Applicants respectfully traverse the assertion in the outstanding Office Action that *Brunner* provides any teaching that could be used to anticipate Claim 2. As a preliminary matter, Applicants respectfully note that Claim 2 was rejected under 35 USC 102(e). However, it is Applicant's understanding that a 102 rejection requires that each limitation in the claim be shown in a single reference, and combining references in a 102 rejection is therefore improper.

Nevertheless, *Brunner* also fails to teach or suggest subject matter that, when combined with *Charron*, would obviate Applicants claimed invention. Even considering *Brunner's* teaching of a checksum and various memory modules to contain the checksum, Applicants respectfully note that *Brunner* does not provide for an independent computation of a binary content verification of the program memory content. In fact, like *Charron*, *Brunner* only discloses a single CPU upon which all computations are dependent. Therefore, even if *Charron* and *Brunner* are combined, Applicants claimed invention does not result because both references fail to teach or suggest independent computing of memory verification.

Applicants respectfully traverse the rejection of Claim 3 as being anticipated by *Charron*. Claim 3 recites:

> ***3. (Original) The method of Claim 1, wherein the step of independently computing the binary content signature comprises storing the binary content signature in a secure memory device.***

However, *Charron* fails to teach or suggest similar subject matter.

Applicants respectfully traverse the assertion in the outstanding that *Charron* discloses *"... storing a binary content signature in a secure memory device."* As discussed above, Applicants respectfully note that *Charron* does not teach or suggest a signature. Further, *Charron's* storage of in an ordinary EEPROM does not constitute a secure memory device because nothing about the *Charron's* memory device makes it secure as only an ordinary EEPROM is described. Accordingly, Applicant respectfully submits that Claim 3 is yet further patentable over *Charron*.

Applicants respectfully submit new Claims 36-73. New Claim 36 recites:

> ***36. (New) A consumer interactive device, comprising:***
>
> ***a processing unit configured to administer use of the consumer interactive device;***
>
> ***a display coupled to the processing unit and utilized by the processing unit to display portions of the use of the consumer interactive device;***
>
> ***a memory unit coupled to the processing unit;***

a set of instructions and/or data for use of the consumer interactive device stored in the memory unit;

a signature calculator independent of the processing unit, the signature calculator coupled to the memory unit and configured to produce a signature from contents of the memory unit;

a signature storage memory coupled to the signature calculator and configured to store a signature produced by the signature calculator; and

a memory unit protection module configured to compare a current signature produced from the current contents of the memory unit, compare the current signature to a previously produced signature and, if the signatures do not match, de-couple the memory unit from the processing unit.

However, the cited references fail to teach or suggest similar subject matter.

Applicants respectfully note that Claim 36 includes *"a signature calculator independent of the processing unit, the signature calculator coupled to the memory unit and configured to produce a signature from contents of the memory unit".* However, none of the cited references teach or suggest a signature calculator independent of the processing unit.

Claim 36 further includes a memory unit protection module that is *"configured to compare a current signature produced from the current contents of the memory unit, compare the current signature to a previously produced signature and, if the signatures do not match, de-couple the memory unit from the processing unit."*and that the memory unit protection is disposed in a secure

memory socket. However, none of the cited references teach or suggest a secure memory socket having similar capability. Therefore, Applicants respectfully submit that Claims 36 and 37 are patentable over the cited references because the cited references fail to teach or suggest subject matter specifically claimed in Claim 36 and/or 37.

Applicants respectfully note new Claim 45 includes a configuration for a casino gaming unit that is entirely unique. Claim 45 recites:

> ***45. A casino gaming unit, comprising:***
>
> ***a processing unit;***
>
> ***a memory unit coupled to the processing unit;***
>
> ***a data read port accessible from a portion of the gaming unit not physically accessible to the memory unit and configured to allow verification of contents of the memory unit.***

However, the cited references fail to teach or suggest similar subject matter.

Applicants respectfully submit that the verification of a memory unit in a casino gaming apparatus without physical access to the memory unit is entirely unique within the gaming industry and very needed feature because of gaming regulations and required memory checks that must be performed on certain time tables to be in compliance with either casino and/or gaming commission rules. In particular, Claim 45 recites a casino gaming unit that includes *"a data read port accessible from a portion of the gaming unit not physically accessible to the memory unit and configured to allow verification of contents of the memory unit,"* however, the cited references fail to teach or suggest similar subject matter. Therefore, Applicants respectfully submit that Claim 45 is patentable over the cited references.

Applicants respectfully note new Claim 52 includes a configuration for a casino gaming apparatus that is entirely unique. Claim 52 recites:

> ***52. A casino gaming apparatus, comprising***

a physically secure, locked, enclosure comprising a processing unit coupled to program memory configured to operate the casino gaming unit, the program memory comprising contents including instructions and/or data utilized by the processing unit;

a program memory verification unit coupled to the program memory and configured to calculate a signature of the program memory contents and verify the calculated signature against the previously calculated signature;

a secure memory, comprising,

an IC memory device physically separated and distinct from the program memory, and accessible only by the program verification unit; and

a Radio Frequency (RF) device coupled to the program verification unit and configured to transmit the verification result to a monitor;

wherein the previously calculated signature is stored in the secure memory.

However, the cited references fail to teach or suggest similar subject matter.

In particular, Applicants respectfully note that Claim 52 includes a second processing unit that calculates signatures from the contents of a program memory and compares the signature to a previously stored signature in a secure memory. Further the secure memory is distinct from the program memory and only accessible to the second processing unit program verification unit. However, the cited references fail to teach or suggest a similar structure. Accordingly, Applicants respectfully submit that Claim 52 is also patentable over the cited references.

Applicants respectfully note new Claim 61 includes a configuration for a casino gaming apparatus that is entirely unique. Claim 61 recites:

> ***61. A secure memory socket, comprising,***
>
> ***a socket device having receptacles positioned to receive pins of a memory unit;***
>
> ***a set of data and control pins coupled to portions of the receptacles and configured to carry data from a memory unit installed in the socket device to a processor device to be coupled to the data and control pins;***
>
> ***a signature calculator coupled to the receptacles and configured to produce a signature from contents of the memory unit,***
>
> ***a signature storage memory coupled to the signature calculator and configured to store a signature produced by the signature calculator, and***
>
> ***a memory unit protection module configured to compare a current signature produced from current contents of the memory unit, compare the current signature to a previously produced signature from the signature storage memory, and, if the signatures do not match, de-couple the receptacles from at least a portion of the pins.***

However, the cited references fail to teach or suggest similar subject matter.

In particular, Applicants respectfully note that Claim 61 is a secure memory socket that is entirely unlike any of the cited references. Accordingly, Applicants respectfully submit that Claim 60 is patentable over the cited references.

Applicants respectfully note new Claim 67 is a method. Claim 67 recites:

67. A method, comprising the steps of:

calculating a first signature from the contents of a program memory in consumer interactive device;

storing the program memory contents signature in a signature memory that is a different and physically separate memory from the program memory;

receiving a command from a Remote Monitor Unit (RMU) to verify contents of the program memory; and

in response to the command,

calculating a second signature from the contents of the program memory,

comparing the first signature to the second signature,

if the signatures do not match, signaling a memory error to the RMU and disabling the program memory from communicating with a processing device utilizing contents of the program memory to operate.

However, the cited references fail to teach or suggest similar subject matter.

In particular, Applicants respectfully note that Claim 67 includes the steps of *"storing the program memory contents signature in a signature memory that is a different and physically separate memory from the program memory;"* and *"if the signatures do not match, signaling a memory error to the RMU and disabling the program memory from communicating with a processing device utilizing contents of the program memory to operate."* However, the cited references fail to teach or suggest the same. Accordingly, Applicants respectfully submit that Claim 67 is patentable over the cited references.

Based on the patentability of independent Claims 1, 36, 45, 52, 61, and 67, Applicants further respectfully submit that dependent Claims 2-10, 37-44, 46-51, 53-60, 62-66, and 68-73 are also patentable.

Consequently, no further issues are believed to be outstanding, and it is respectfully submitted that this case is in condition for allowance. An early and favorable action is respectfully requested.

Respectfully submitted,
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